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Inventor(s): Ken YAMAUCHI

For: METHOD AND APPARATUS FOR DECODING THE DATA, DATA RECEIVING SYSTEM, AND DATA TRANSMITTING AND RECEIVING SYSTEM

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Respectfully submitted,

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC

By: Charles M. Marmelstein
Reg. No. 25,895

1050 Connecticut Avenue, N.W.
Suite 600
Washington, D. C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

CMM:mmg

METHOD AND APPARATUS FOR DECODING THE DATA, DATA RECEIVING SYSTEM, AND DATA TRANSMITTING AND RECEIVING SYSTEM

FIELD OF THE INVENTION

The present invention relates to a technology of demodulating a received digital-modulated signal and decoding actual data from digital data obtained by the demodulation. More particularly, the invention relates to a decoding method, a decoder, a data receiving system, and a data transmission and receiving system which decode a data stream, which is coded by using a convolutional code and is multiplexed in time division, using Viterbi decoding.

BACKGROUND OF THE INVENTION

Recently, as integrated circuits and coding techniques, which can process digital data at a high speed, develop are becoming available. Therefore, analog-system techniques are now replaced by such digital techniques. Particularly, growth in the communication field is remarkable. For example, television broadcasting service, satellite broadcasting service and the like are being converted to digital broadcasting.

The digital satellite broadcasting adopts a radio communication system in which a carrier signal is transmitted via an artificial satellite and is received directly by a

receiver installed in a house or the like. However, since this digital satellite broadcasting utilizes the atmosphere as a transmission space, it is easily influenced by weather and the other factors. When the weather is bad the reception becomes worse. As a result, in a transmitter and a receiver which are terminal sections of the digital satellite broadcasting system, the transmission/receiving process with high stability and high reliability is required in comparison with the conventional cable and ground wave television service.

In radio communication of a digital-modulated signal like the digital satellite broadcasting, digital data to be digital-modulated are composed of bit strings (data stream) which undergo a so-called coding process in which redundancy is added to actual data so that the stability and reliability of the transmission/receiving process is heightened.

As the redundancy of the data stream is higher, error correction ability of the data stream is improved further in the decoding process in the receiver. In other words, even if the data stream with high redundancy include a lot of error bits upon receiving, the error bits can be corrected and the data stream can be reproduced correctly upon transmission. Meanwhile, such data stream with high redundancy has a disadvantage that a number of structure bits increases and transmission efficiency is lowered.

When image or sound information is received as data stream including a little error, for example, the information as a

whole can be accepted. Therefore, the redundant may be comparatively lowered and the transmission efficiency heightened so that a lot of information can be transmitted. On the other hand, for a data stream which represents computer programs where even one bit error is not allowed, generally the redundancy is set to comparatively higher value because upon receiving the information is required to be securely restored.

Fig. 1 is a block diagram showing a schematic structure of a conventional transmitter and particularly shows a portion of the transmitter used in digital satellite broadcasting. This transmitter is composed of a coder 100 and a modulator 150. The coder 100 multiplexes and codes data from a plurality of information sources 1, 2, ···, n. The modulator 150 modulates the coded signals according to a predetermined modulation system. The information sources here are digital data strings (transport stream) which are compressed by MPEG2 (Motion Picture Expert Group 2) as one of the motion picture compressing systems.

Further, the coder 100 is composed of a multiplexer 110, a convolution coder 120, a punctured module 130 and a multiplex control signal generator 140. Although not shown in the figure, the multiplexer 110 is composed of, for example, a Reed-Solomon coding circuit, a frame structure circuit, an energy dispersion circuit and an interleaver and multiplexes and codes the input information sources. Operation of the transmitter is explained below.

The multiplex control signal generator 140 generates a multiplex control signal which represents multiplexed information of the information sources. The multiplexed information is the information which represents positions (timing) of information source data multiplexed on one carrier and transmission systems (redundancy, modulation systems, etc).

The information sources are input into the Reed-Solomon coding circuit of the multiplexer 110. The Reed-Solomon coding circuit adds a Reed-Solomon code which, can correct an error of a byte unit in the receiver based on the multiplex information represented by the multiplex control signal output from the multiplex control signal generator 140, to the bit strings of the information sources so as to output the coded strings of the respective information sources.

The code strings output from the Reed-Solomon coding circuit are input into the frame structure circuit. The frame structure circuit multiplexes the code strings based on the multiplex information represented by the multiplex control signal output from the multiplex control signal generator 140 so as to structure a frame to be a unit of the multiplexed data.

A signal output in the frame unit from the frame structure circuit is input into the energy dispersion circuit. The energy dispersion circuit adds (scramble) a pseudo random signal (energy dispersion signal) to the digital data. As a result, the digital data composing the input frames, namely, bit strings

are not transmitted as enumeration of bit "0" or bit "1" for long period.

The aim is to prevent misconception of reception such as error detection or non-detection of a digital signal on the receiving side due to reception of the long-period continuous same bits. The pseudo random signal should be removed on the receiving side. For this reason, also in the energy dispersion circuit, a position of the digital data, where information representing a generating condition of the pseudo random signal such as a random initial value and the like is shown, is determined by referring to the multiplex information.

The signal scrambled in the energy dispersion circuit is input into the interleaver. The interleaver rearranges the digital data represented by the input signal in byte unit so as to improve resistance to a burst error (long-period continuous error) appearing intensively in time.

As a result, even if burst errors occur in the rearranged digital signals, the errors which occur intensively can be dispersed because the process for restoring the rearrangement of the digital signals (the process by the interleaver) is executed on the receiving side. As a result, improvement of the error correction and a correct recognition rate of the transmitted information can be heightened. The information about the rearrangement can be obtained also from the multiplex information.

The signals arranged by the interleaver are the outputs

of the multiplexer 110 and are input into the convolution coder 120. The convolution coder 120 executes the convolution coding process with respect to the input signals. As a result, random errors such as errors of irregular bit units such as a thermal noise which are generated in a transmission line or the receiver can be corrected.

Fig. 2 is a block diagram showing a schematic structure of the convolution coder 120. The convolution coder 120 is composed of a shift register comprising D latches 121 and 122, two EXOR circuits 124 and 125, and a parallel-serial converter 128. The convolution coder 120 executes the coding in such a manner that one-bit input data are output as 2-bit data. When the coding rate is defined as (Original information content) / (coded information content), the coding rate in the convolution coder 120 is 1/2.

In the convolution coder 120 shown in Fig. 2, two-bit serial data are held by the D latches 121 and 122 in the order of input. Three-bit serial data are converted into parallel data by the two-bit data and one-bit data further input. Newly input data and the data held in the D latches 121 and 122 are input into the EXOR circuit 124 so as to undergo exclusive OR. Moreover, the newly input data and the data held in the D latch 122 are input into the EXOR circuit 125 so as to undergo exclusive OR.

The calculated results of the two exclusive OR are again converted into serial data in the parallel-serial converter 128.

As a result, three-bit input serial data are output as six-bit serial data, for example, and this output result becomes a convolution code.

In order to improve the transmission efficiency, four-bit data, which are obtained by thinning out two bits from six-bit data output from the convolution coder 120, are used as output data. In this method, the coding rate is 3/4, and in comparison with the coding rate 1/2 in the case of the convolution coder 120, redundancy can be made lower and the transmission efficiency can be heightened.

Furthermore, this method simultaneously reduces the error correction ability. As a result, the redundancy can be controlled by changing a degree of the thinning-out of data. This data thinning-out process is called as puncturing. The punctured module 130 shown in Fig. 1 executes such puncturing.

Fig. 3 is an explanatory diagram showing an example of the coding rate obtained by puncturing. Fig. 3 shows puncturing of the coding rates 2/3, 3/4, 5/6 and 7/8 which is generated by thinning out a convolution code of the coding rate 1/2. Explanation is provided below for the puncturing of the coding rate 3/4.

It is assumed that data "x0, y0, x1, y1, x2, y2" are obtained from data constituted by "d0, d1, d2" by the convolution coder 120. In such a case, the punctured module 130 deletes a bit in a position corresponding to "0" with reference to a previously prepared bit deletion map "1, 1, 0,

1, 1, 0". Undeleted bit after the deleted one is shifted to the position of the deleted bit. In other wards, this bit deletion map shows that two bits are thinned out from six bits. As a result, only four-bit data of "x0, y0, y1, x2" are output.

Thus, the punctured module 130 enables changes of various kinds in the coding rates as shown in Fig. 3. When a various kinds of bit deletion maps are prepared, the transmission efficiency can be selected according to a signal transmission line or a signal characteristic.

The code strings output from the punctured module 130 in such a manner become a data stream which is obtained by coding and multiplexing data of a plurality of information sources with the coding rates determined in the respective information source. The data stream is output from the coder 100. The data stream is input into the modulator 150 shown in Fig. 1 and is digital-modulated according to a modulation system which is suitable to the carrier so as to be output as a transmission signal.

As the digital modulation executed in the modulator 150, modulations like amplitude modulation (ASK), frequency modulation (FSK), phase modulation (PSK) may be considered. An explanation is provided below for the digital phase modulation.

The digital phase modulation is a system where the bit structures composed of "0" or "1" of the digital data are made to have correspondence to phases, and the phases are changed for the carrier so that information is transmitted. The digital

phase modulation system further includes BPSK, QPSK (or 4PSK), 8PSK and the like according to a number of phases to be used.

As for the transmission signal which is digital-phase modulated, one phase state (transmission symbol) of the carrier is checked in the receiver so that one-bit information can be transmitted in BPSK and two-bit information in QPSK and three-bit information in 8PSK. This shows that the transmission efficiency varies with the respective phase modulation systems. However, as the transmission efficiency becomes higher, adjacent transmission symbols are closer to each other so that clear distinction between the phases becomes difficult. As a result, error can be easily generated in the information. For this reason, the phase modulation using these three systems is selected according to a characteristic of information to be transmitted.

In other words, as for the data of the information sources multiplexed as the data stream, in addition to the selection of the coding rates by means of the coder 100, the modulation system by means of the modulator 150 can be selected.

Fig. 4 is an explanatory diagram showing a structure of the data stream output from the coder 100. The data stream shown in Fig. 4 is generated by the frame structure circuit. A data stream 1, a data stream 2, and a data stream 3 which represent three information source data are multiplexed and arranged in a frame identified by a synchronous code. For example, the data stream 1, the data stream 2, and the data stream 3 can be

allocated in this order to a QPSK modulation stream of the coding rate 3/4, a QPSK modulation stream of the coding rate 1/2 and a BPSK modulation stream of the coding rate 1/2.

In addition, some frames can be processed as one collective information (hereinafter, referred to as "super frame"). In this case, in the super frame composed of eight frames, for example, the synchronous code is arranged at the head of each frame, and a parity signal corresponding to the Reed-Solomon code is arranged in the last two frames so that the error correction ability is heightened.

An explanation is provided below for a conventional receiver which receives a transmission signal transmitted from the transmitter and demodulates and decodes the signal. Fig. 5 is a block diagram showing a schematic structure of such a conventional receiver. Fig. 5 shows one example of the receiver of the digital satellite broadcasting which is suitable to the transmitter in Fig. 1. This receiver is composed of a demodulator 190 further having a digital phase modulation circuit and a decoder 200.

The decoder 200 is composed of a depuncture module 210, a Viterbi decoder 220, a synchronizer 230, a data stream decoder 240, a multiplex control signal generator 250, and a multiplex information storage section 260. The data stream decoder 240 is composed of, for example, a deinterleaver, an energy dispersion signal removal circuit and a Reed-Solomon code error correcting circuit correspondingly to the similar structure in

the multiplexer 110 shown in Fig. 1. The data stream decoder 240 decodes the multiplexed data stream. Operation of this receiver is explained below.

Similarly to the multiplex control signal generator 140 shown in Fig. 1, a multiplex control signal is generated in the multiplex control signal generator 250 of the decoder 200. Multiplex information represented by the multiplex control signal is previously stored in the multiplex information storage section 260. The multiplex control signal generator 250 generates a multiplex control signal based on the multiplex information.

The demodulator 190 demodulates the received signal in accordance with acquisition timing of the information source data represented by the multiplex control signal and the modulation system. Precisely, the demodulator 190 extracts a code string in the state before the received signal is modulated in the modulator 150 of the transmitter, and digital phase demodulation is executed in this example.

The signal demodulated by the demodulator 190 is input into the depuncture module 210 of the decoder 200. The depuncture module 210 inserts the bit which is deleted in the punctured module 130 into the input signal based on the coding rate represented by the multiplex control signal (depuncturing).

The code string which is depunctured by the depuncture module 210 is input into the Viterbi decoder 220 so that the

convolutional code coded in the convolution coder 120 of the transmitter is decoded. That is, the Viterbi decoder 220 calculates a Hamming distance between the code represented by the input code string and a code on a trellis chart as path metric and leaves path metric of short Hamming distance as survival path. Further, the Viterbi decoder 220 decodes a code string corresponding to a path metric of the shortest Hamming distance as a maximum code.

The code string decoded by the Viterbi decoder 220 is input into the synchronizer 230. The synchronizer 230 detects a synchronous code in the frame shown in Fig. 4 from the data stream and generates a control signal for acquiring the decoding timing of the multiplexed code strings.

Fig. 6 is a block diagram showing a schematic structure of the synchronizer 230. As shown in Fig. 6, the received code string is input into a sync word detection circuit 231 and a buffer 235. The sync word detection circuit 231 detects the synchronous code from the input code string and generates a detection signal. The synchronous acquisition control circuit 232 outputs a signal representing synchronous timing according to the received the detection signal and a predetermined synchronous clock.

A control signal generation circuit 233 inputs the signal output from the synchronous acquisition control circuit 232 so as to output a control signal representing that current time is positioned at the head of the frame. Meanwhile, the code

string input into the buffer 235 is delayed until output of the control signal is completed so as to be output as data stream at predetermined timing. The control signal output from the synchronizer 230 is input into the multiplex control signal generator 250 shown in Fig. 5 so as to be utilized for obtaining output timing of the multiplex control signal.

The data stream output from the synchronizer 230 is input into the data stream decoder 240. The data stream then undergoes the decoding processes corresponding to the coding processes in the interleaver, the energy dispersion circuit and the Reed-Solomon coding circuit composing the multiplexer 110 shown in Fig. 1.

The decoded data bit string output from the data stream decoder 240 becomes an output of the decoder 200 and is input into a not shown MPEG reproduction apparatus or the like, which is connected in the later stage. This MPEG reproduction apparatus extracts corresponding data from the data bit string by selecting an information source, and displays the extracted data as a motion picture.

However, as mentioned above, the transmission-reception system composed of the convolution coder 120 and the Viterbi decoder 220, coding and decoding are executed by the calculation methods based on superposing of past bit strings continuously transmitted. For this reason, a data stream having coding rate of high error correction ability is influenced by the case that error cannot be corrected in a data stream having coding rate

of low error correction ability. As a result, the whole error correction ability of the multiplexed data stream is lowered.

For example, consider a case in which two or more kinds of coding rates are used between the data streams composing the multiplexed data stream, and comparatively big noise is mixed on the transmission line. In this case, although error can be sufficiently corrected in the data stream having coding rate of high error correction ability in the multiplexed data streams, error is still included in a decoded result of the data stream having coding rate of low error correction ability. In this state, the Viterbi decoder decodes the data stream having coding rate of high error correction ability which is next input continuously according to calculation of path metric using the data stream including the error. For this reason, the data stream having coding rate of high error correction ability cannot be decoded correctly.

In order to solve such a problem, Japanese Patent Application Laid-Open No. 9-247003 discloses "information receiver". This information receiver inserts a known "end bit" into a plurality of multiplexed data streams by means of the convolution coder just before the coding rate changes. The Viterbi decoder initializes path metric at timing that the "end bit" is detected.

As a result, in the state that the path metric is initialized per data stream, namely in the state that a storage device of a Hamming distance calculated in the Viterbi decoder

is initialized, Viterbi decoding can be started. This prevents the data streams having different coding rates from being influenced by the decoding.

However, the "information receiver" cannot solve the above problem when the "end bit" cannot be inserted into the data streams from the viewpoint of the standard of data transmission in digital satellite broadcasting or the like. If the "end bit" is not inserted and not detected and the path metric is initialized at a change point of the coding rate, namely, a point that transmission of next data stream is started, there arises a new problem that a convolutional code fails and the error correction ability is lowered.

For example, in a data stream which is obtained by multiplexing a code of low error correction ability and a code of high error correction ability, an error of a code having low error correction ability which can be corrected sufficiently occurs on a transmission line. In this case, when the path metric is initialized at the change point of the data stream, a vicinity of the head of the data stream cannot be decoded. As a result, more errors occur than the case that the initialization is not executed.

SUMMARY OF THE INVENTION

It is an object of the invention to initialize path metric in a Viterbi decoder according to strength of a noise on a transmission line and coding rates of continuous data streams

so as to optimally decode a plurality of data stream, which are multiplexed without inserting an "end bit" thereinto, with high stability and reliability.

In order to solve the above problem and achieve the above object, in a decoding method and a decoder of the present invention a signal-to-noise ratio monitor measures the strength of the noise included in the multiplex data, and a comparison unit outputs a post signal when the measured noise strength is equal to or greeter than a preset value, and an initialization signal generation unit inputs an initialization signal into the Viterbi decoder at timing that decoding of the data streams is started according to the receipt of the post signal so that calculated path metric is initialized.

Thus, only when the noise which exceeds a predetermined value is detected by the signal-to-noise ratio monitor, the path metric of the Viterbi decoder is initialized. For this reason, only in the case where a noise where an initializing effect can be obtained even after adding deterioration of the decoding characteristic due to the initialization occurs, the initialization is possible.

Further, a signal selection unit initializes path metric of the Viterbi decoder only when a coding rate of a data stream to be decode is larger than a coding rate of a data stream which has just been decoded.

Thus, only when the timing that the initialization signal is input is the point that the data stream having coding rate

of low error correction ability is changed into the data stream having coding rate of high error correction ability, the Viterbi decoder is initialized. For this reason, the calculated result of the path metric calculated by decoding the data stream having coding rate of high error correction ability can be utilized when the next data stream having coding rate of low error correction ability is decoded.

Other objects and features of this invention will become apparent from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a schematic structure of a conventional transmitter.

Fig. 2 is a block diagram showing a schematic structure of a convolution coder in the conventional transmitter.

Fig. 3 is an explanatory diagram showing an example of a coding rate obtained by puncturing in the conventional transmitter.

Fig. 4 is an explanatory diagram showing a structure of a data stream output from a conventional coder.

Fig. 5 is a block diagram showing a schematic structure of a conventional receiver.

Fig. 6 is a block diagram showing a schematic structure of a synchronizer in the conventional receiver.

Fig. 7 is a block diagram showing a schematic structure

of a decoder according to a first embodiment.

Fig. 8 is a block diagram showing another schematic structure of the decoder according to the first embodiment.

Fig. 9 is a block diagram showing a schematic structure of the decoder according to a second embodiment.

Fig. 10 is a block diagram showing a schematic structure of the decoder according to a third embodiment.

Fig. 11 is an explanatory diagram showing a structure of a data stream which is decoded in the decoder according to a fourth embodiment.

Fig. 12 is a block diagram showing a schematic structure of the decoder according to the fourth embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of a decoding method and a decoder of the present invention are explained below with reference to the attached drawings. However, this invention is not limited to these embodiments.

A decoding method and a decoder according to a first embodiment is explained here. The decoding method and the decoder according to the first embodiment have the following characteristic in addition to the characteristic of the conventional decoder 200. Precisely, noise strength of a signal output from the demodulator 190 is measured and when the measured noise strength exceeds a predetermined value only then an initialization signal which instructs initialization of path

metric is input into the Viterbi decoder 220 via the multiplex control signal generator 250. As a result, decoding can be executed optimally in accordance with the strength of the noise mixed on the transmission line.

Fig. 7 is a block diagram showing a schematic structure of the decoder according to the first embodiment. The decoder 10 shown in Fig. 7 is provided with a signal-to-noise ratio monitor 12 and a comparator 14. The signal-to-noise ratio monitor 12 measures strength of noise from a signal input into the depuncture module 210 so as to digitize the measured noise strength. The comparator 14 compares the output of the signal-to-noise ratio monitor 12 with a predetermined value and outputs a signal representing the result of comparison (hereinafter, referred to as a post signal). The multiplex control signal generator 250 outputs an initialization signal to the Viterbi decoder 220 based on the post signal received from the comparator 14. This process is different from the one executed in the conventional decoder 200.

The legends same as in Fig. 5 are provided to the other components which are common to those of the conventional decoder 200, and the explanation thereof is omitted. The Viterbi decoder 220 initializes an internal Hamming distance storage device according to an external signal.

Operation of the decoder 10 will be now explained. A signal output from the demodulator 190 or the like shown in Fig. 5 is input into the depuncture module 210 and the signal-

to-noise ratio monitor 12. The signal-to-noise ratio monitor 12 measures noise strength of BER (Bit Error Rate) or the like with predetermined time intervals from the input signal so as to output the measured result as a measurement signal. The measurement signal output from the signal-to-noise ratio monitor 12 is input into the comparator 14 so as to be judged as to whether or not a noise is allowable.

It is assumed that a value which represents an upper limit of the allowable noise has been previously set in the comparator 14. When the value of the measurement signal exceeds this set value, a low-level pulse signal is output as a post signal, for example. Moreover, when the value of the measurement signal does not exceed the set value, a signal in a high-level state is output.

Meanwhile, the signal input into the decoder 10 is input into the depuncture module 210, the Viterbi decoder 220, the synchronizer 230 and the data stream decoder 240 successively so as to undergo the decoding processes. A control signal generated by the synchronizer 230 is fed back to the multiplex control signal generator 250. The control signal is used for taking timing of a multiplex control signal which decodes respective data streams according to multiplex information in the depuncture module 210 and the data stream decoder 240.

The multiplex control signal generator 250 receives the post signal output from the comparator 14 thereinto. When the post signal represents the state that the value exceeds the set

value, namely, a big noise is mixed in the received signal, the initialization signal is output at timing based on the control signal output from the synchronizer 230, namely, timing that decoding of the respective data streams is started.

The initialization signal is input into the Viterbi decoder 220. The Viterbi decoder 220 initializes Hamming distances which have been calculated and stored, namely, path metrics according to the input of the initialization signal. As a result, an influence of the superposed noise in the decoding of the code string in the previous position can be avoided.

There arises a problem here that reliability of the maximum judgment of Viterbi decoding is lowered at the first stage of the data stream because the path metric is initialized. However, in the state that a noise of not less than certain strength is mixed in the received signal, it was confirmed by an experiment conducted by the inventors that more accurate decoding can be executed by such initialization process. Therefore, it is necessary to set the set value in the comparator 14 as a threshold value as to whether or not an effect is produced when the initializing process is carried out.

The set value in the comparator 14 can be changed with an external signal by providing a register. Fig. 8 is a diagram showing a schematic structure in the case where the register is provided in the decoder according to the first embodiment. The register 22 stores and holds the set value. The comparator 14 refers to the set value stored in the register 22 so as to

be capable of changing the post signal to be input into the multiplex control signal generator 250, namely, an initializing condition according to the a condition of the transmission line and a code to be received.

In the decoders 10 and 20, the signal-to-noise ratio monitor 12 may measure noise strength for a modulated signal output from the modulator, not shown. Further, the signal-to-noise ratio monitor 12 may measure noise strength for a received signal to be input into the demodulator.

Further, an initialization signal generator may be provided instead of the multiplex control signal generator 250 to generate the initialization signal.

The decoding method and the decoder according to the first embodiment measures the strength of noise mixed in the received signal in the transmission system which transmits and receives data composed of multiplexed data stream. When the noise has a value which is equal to or greater than the predetermined set value, the initialization signal representing the initialization of the path metric is input into the Viterbi decoder 220 at a predetermined timing. For this reason, the decoded result with high reliability can be obtained in comparison with the decoded result obtained in the case where a comparatively big noise is mixed in the received signal.

Particularly according to the decoding method and the decoder of the first embodiment, in the case where a noise that error cannot be corrected sufficiently at the low coding rate

is generated, secure decoding with originally high error correction ability can be executed in the data stream having the high coding rate without being influenced by the noise.

A decoding method and a decoder according to a second embodiment will be now explained. The decoding method and the decoder according to the second embodiment have the following characteristic in addition to the characteristic of the decoder 20 according to the first embodiment. Precisely, the initialization signal is input into the Viterbi decoder 220 only at a point that the data stream having coding rate of low error correction ability is changed into the data stream having coding rate of high error correction ability.

Fig. 9 is a block diagram showing a schematic structure of the decoder according to the second embodiment. The decoder 30 is provided with a signal selector 32. The signal selector 32 outputs the initialization signal to the Viterbi decoder 220 based on the multiplex information stored in the multiplex information storage section 260. The presence and absence of this signal selector 32 is the difference between the decoder 20 shown in Fig. 8 and the decoder 30. Legends same as in Fig. 8 are provided to the other components which are common to those of the decoder 20 according to the first embodiment, and the explanation thereof is omitted.

Operation of the decoder 30 will be explained below by taking into consideration only the differences with respect to the first embodiment. In Fig. 9, it is assumed that a post

signal which represents that the noise exceeds the set value is output by the comparator 14 to the multiplex control signal generator 250. The multiplex control signal generator 250 outputs the initialization signal at a timing of the control signal output by the synchronizer 230. The initialization signal is input into the signal selector 32. The signal selector 32 also receives the multiplex information stored in the multiplex information storage section 260. The signal selector 32 then judges as to the timing that the initialization signal is input shows a point that which data stream is changed into which data stream.

Particularly, when the signal selector 32 judges that the timing that the initialization signal is input is the point that the data stream having coding rate of low error correction ability is changed into the data stream having coding rate of high error correction ability, only then the initialization signal is allowed to pass to the Viterbi decoder 220.

In the decoding of the data stream having coding rate of high error correction ability, an error can be corrected sufficiently even in a signal into which a comparatively big noise is mixed. As a result, coding of the next data stream having coding rate of low error correction ability is not influenced. On the contrary, if the initialization is executed at this change point, the decoding characteristic is deteriorated.

The signal selector 32 is provided so as to prohibit the

Viterbi decoder 220 from being initialized at the point that the data stream having coding rate of high error correction ability is changed into the data stream having coding rate of low error correction ability.

The decoding method and the decoder according to the second embodiment initialize the Viterbi decoder 220 in the transmission system which transmits and receives data composed of multiplexed data stream at the point that the strength of noise mixed in the received signal exceeds the predetermined value and the data stream having coding rate of low error correction ability is changed into the data stream having coding rate of high error correction ability. As a result, the coded result with high reliability which is not much influenced by the noise can be obtained.

A decoding method and a decoder according to a third embodiment will be now explained. The decoding method and the decoder according to the third embodiment have the following characteristic in addition to the characteristic of the decoder 30 according to the second embodiment. Precisely, a plurality of multiplexed data stream are extracted from the data stream decoded by the data stream decoder 240 so as to be distributed.

Fig. 10 is a block diagram showing a schematic structure of the decoder according to the third embodiment. This decoder 40 is provided with a distribution device 42, which distributes the plurality of data stream composing the data stream, at the later stage of the data stream decoder 240. This point is

different from the decoder 30 shown in Fig. 9. Legends same as in Fig. 9 are provided to the other components which are common to those of the decoder 30 according to the second embodiment, and the explanation thereof is omitted. The multiplex control signal generator 250, in addition to other functions, generates a signal representing distribution timing of the data streams by means of the distribution device 42.

The multiplexed data streams are selected from the data stream decoded by the data stream decoder 240 so as to be distributed in the apparatus to which the decoders 10, 20 and 30 are connected. In this case, this apparatus to which the decoders are connected has to hold multiplex information and generate a multiplex control signal by means of the circuit configuration corresponding to the multiplex control signal generator 250 and the multiplex information storage section 260.

The distribution device 42 is provided at the later stage of the data stream decoder 240 in the decoder 40 so that the circuit configuration of the whole receiver equipped with this decoder 40 can be simplified. Signals which change punctured codes and the like already exist in the multiplex control signal generator 250 or the like in the decoder 40. Therefore, it is easy to generate a signal which distributes information.

The decoding method and the decoder according to the third embodiment initialize the Viterbi decoder 220 in the transmission system which transmits and receives data composed

of multiplexed data stream at the point that the strength of noise mixed in the received signal exceeds the predetermined value and the data stream having coding rate of low error correction ability is changed into the data stream having coding rate of high error correction ability. Further, the distribution device 42 which distributes multiplexed data streams is provided at the later stage of the data stream decoder 240. As a result, the effect of the second embodiment can be produced, and the circuit configuration of the whole receiver equipped with the decoder 40 can be simplified.

A decoding method and a decoder according to a fourth embodiment will be now explained. In the decoders 10, 20, 30 and 40 according to the first to third embodiments, the multiplex information is known in the receiving side and is previously stored in the multiplex information storage section 260. However, the decoding method and the decoder according to the fourth embodiment is characterized in that the multiplex information is included in the transmission signal transmitted from the transmitter and the decoding process is executed dynamically upon receiving the multiplex information.

Fig. 11 is an explanatory diagram showing a structure of the data stream which is decoded by the decoder according to the fourth embodiment. As shown in Fig. 11, as for the signal which is input into the decoder according to the fourth embodiment via the demodulator, not shown, the multiplex information detected by a synchronous code 1 and the multiplexed

data streams 1 to 3 detected by a synchronous code 2 are arranged in one frame, for example.

Fig. 12 is a block diagram showing a schematic structure of the decoder according to the fourth embodiment. This decoder 60 is provided with a multiplex information decoder 64 which decodes the multiplex information. This is different from the decoder 40 shown in Fig. 10. Legends same as in Fig. 10 are provided to the other components which are common to the decoder 40 according to the third embodiment, and the explanation thereof is omitted. The multiplex information storage section 260 receives a signal which represents the multiplex information output from the multiplex information decoder 64 so as to rewrite the multiplex information to be stored based on the input signal.

Operations of the decoder 60 which are different from those in the third embodiment will only be explained here. A plurality of information source data are coded by a system composed of the Reed-Solomon coding circuit, the frame structure circuit, the energy dispersion circuit and the interleaver in the multiplexer 110 of the coder 100. Moreover, the multiplex information is coded by the Reed-Solomon coding circuit and the energy dispersion circuit, and a synchronous code is added to the information source data and the multiplex information and they are multiplex. As a result, the data stream output from the coder of the transmitter is obtained.

The synchronizer 62, in the same manner as shown in Fig.

6, generates a control signal to be input into the multiplex control signal generator 250. Moreover, the synchronizer 62 extracts the data stream and the data stream representing the multiplex information from the input signal.

The data stream extracted in the synchronizer 62 is input into the data stream decoder 240 so as to undergo the decoding process. Meanwhile, the data stream representing the multiplex information in the synchronizer 62 is input into the multiplex information decoder 64. Although not shown in this figure, the multiplex information decoder 64 is composed of an energy dispersion signal removal circuit and a Reed-Solomon code error correcting circuit. The multiplex information decoder 64 decodes the multiplex information from the input data stream.

The multiplex information decoded in the multiplex information decoder 64 is input as a multiplex information signal into the multiplex information storage section 260. The multiplex information storage section 260 updates the stored multiplex information into multiplex information represented by this multiplex information signal. The multiplex information stored in the multiplex information storage section 260 is referred to by the multiplex control signal generator 250.

The decoding method and the decoder according to the fourth embodiment initialize the Viterbi decoder 220 in the transmission system which transmits and receives data composed

of multiplexed data stream at the point that the strength of noise mixed in the received signal exceeds the predetermined value and the data stream having coding rate of low error correction ability is changed into the data stream having coding rate of high error correction ability. Further, the multiplex data stream is distributed, and in the case where the multiplex information is included in the received signal, the multiplex information is decoded so that the decoding form of the respective multiplexed data streams can be changed dynamically. As a result, in the case where the transmission signal where the multiplex form is changed is decoded, the effect of the third embodiment can be produced.

As explained above, according to the present invention, when the signal-to-noise ratio monitor detects that the noise exceeds a predetermined value, only then the path metric of the Viterbi decoder is initialized. For this reason, only in the case where a noise where an initializing effect can be obtained even after adding deterioration of the decoding characteristic due to the initialization occurs, the initialization is possible. As a result, the optimal decoding with high stability and reliability can be executed in comparison with the decoding which is executed in the case where a comparatively big noise is mixed in the received signal.

Furthermore, when the timing that the initialization signal is input is the point that the data stream having coding rate of low error correction ability is changed into the data

stream having coding rate of high error correction ability, only then the Viterbi decoder is initialized. For this reason, the calculated result of the path metric calculated by decoding the data stream having coding rate of high error correction ability can be utilized when the next data stream having coding rate of low error correction ability is decoded. As a result, the high-reliable decoded result which is not much influenced by noise can be obtained.

Although the invention has been described with respect to a specific embodiment for a complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modifications and alternative constructions that may occur to one skilled in the art which fairly fall within the basic teaching herein set forth.

WHAT IS CLAIMED IS:

1. A decoding method of decoding multiplex data using the Viterbi decoding method, which multiplex data are composed by multiplexing a plurality of data stream in time division, which data streams are coded by at least convolution code and whose coding rates and modulation systems are set respectively, the decoding method comprising the steps of:

measuring the strength of the noise contained in the multiplex data;

checking whether the measured noise strength is equal to or greater than a predetermined value; and

when the measured noise strength is equal to or greater than the predetermined value, initializing the path metric calculated based on the Viterbi decoding method at a timing at which the decoding of individual data streams is started.

2. The decoding method according to claim 1, wherein when the coding rate of the data stream to be decoded is larger than a coding rate of the data stream which has just been decoded, only then the path metric is initialized.

3. A data receiving system comprising:

a Viterbi decoder which decodes multiplex data composed by multiplexing a plurality of data stream in time division, which data streams are coded by at least convolution code and whose coding rates and modulation systems are set respectively;

a signal-to-noise ratio monitor which measures the strength of the noise included in the multiplex data;

a comparison unit which checks whether the measured noise strength is equal to or greater than a predetermined value and outputs a notification signal when the measured noise strength is equal to or greater than the predetermined value; and

an initialization signal generation unit which outputs an initialization signal which initializes the path metric calculated in said Viterbi decoder at a timing at which the decoding of individual data streams is started when receiving the notification signal.

4. The data receiving system according to claim 3 further comprising a signal selection unit which,

receives the initialization signal,

checks whether a code rate of the data stream to be decoded is larger than a coding rate of the data stream which has just been decoded, and

provides the initialization signal to said Viterbi decoder when the code rate of the data stream to be decoded is larger than the coding rate of the data stream which has just been decoded.

5. The data receiving system according to claim 3 further comprising a distribution unit which distributes the multiplex data after the multiplex data are decoded and outputs the

distributed data.

6. The data receiving system according to claim 3 further comprising a multiplex information decoding unit which extracts multiplex information from multiplex data so as to decode the multiplex information when the multiplex data has multiplex information as an added information.

7. The data receiving system according to claim 3, wherein said predetermined value is variable.

8. The data receiving system according to claim 3, wherein said data stream is BPSK, QPSK or 8PSK.

9. A decoder comprising:

a Viterbi decoder which decodes multiplex data composed by multiplexing a plurality of data stream in time division, which data streams are coded by at least convolution code and whose coding rates and modulation systems are set respectively;

a signal-to-noise ratio monitor which measures the strength of the noise included in the multiplex data;

a comparison unit which checks whether the measured noise strength is equal to or greater than a predetermined value and outputs a notification signal when the measured noise strength is equal to or greater than the predetermined value; and

an initialization signal generation unit which outputs

an initialization signal which initializes the path metric calculated in said Viterbi decoder at a timing at which the decoding of individual data streams is started when receiving the notification signal.

10. A data transmitting and receiving system comprising:

a transmitting unit which transmits a time division multiplexing data including a plurality of data stream; and

a receiving unit which receives and decodes the time division multiplexing data,

said receiving unit comprising,

a Viterbi decoder which decodes said time division multiplexing data;

a signal-to-noise ratio monitor which detects the noise in the time division multiplexing data; and

an initialization signal generating unit which outputs a initialization signal to said Viterbi decoder on the basis of the detected noise so as to initialize the path metric calculated by said Viterbi decoder at a timing when decoding of each of said plurality of data stream is started.

11. The data transmitting and receiving system according to claim 10, wherein the initialization signal is outputted to said Viterbi decoder when the coding rate of the data stream to be decoded is lager than that of the data stream decoded before.

ABSTRACT OF THE DISCLOSURE

A plurality of data stream, which are coded by a convolution code and where coding rates and modulation systems are set respectively, are multiplexed in time division so that multiplex data are composed. A signal-to-noise ratio monitor measures the strength of the noise included in the multiplex data. A comparator outputs a post signal when a comparison indicates that the measured noise strength is equal to greater than a preset value. A multiplex control signal generator inputs an initialization signal into a Viterbi decoder at a timing at which decoding of individual data streams is started based on the received post signal. The Viterbi decoder initializes the calculated path metric upon receipt of the initialization signal.

FIG.1

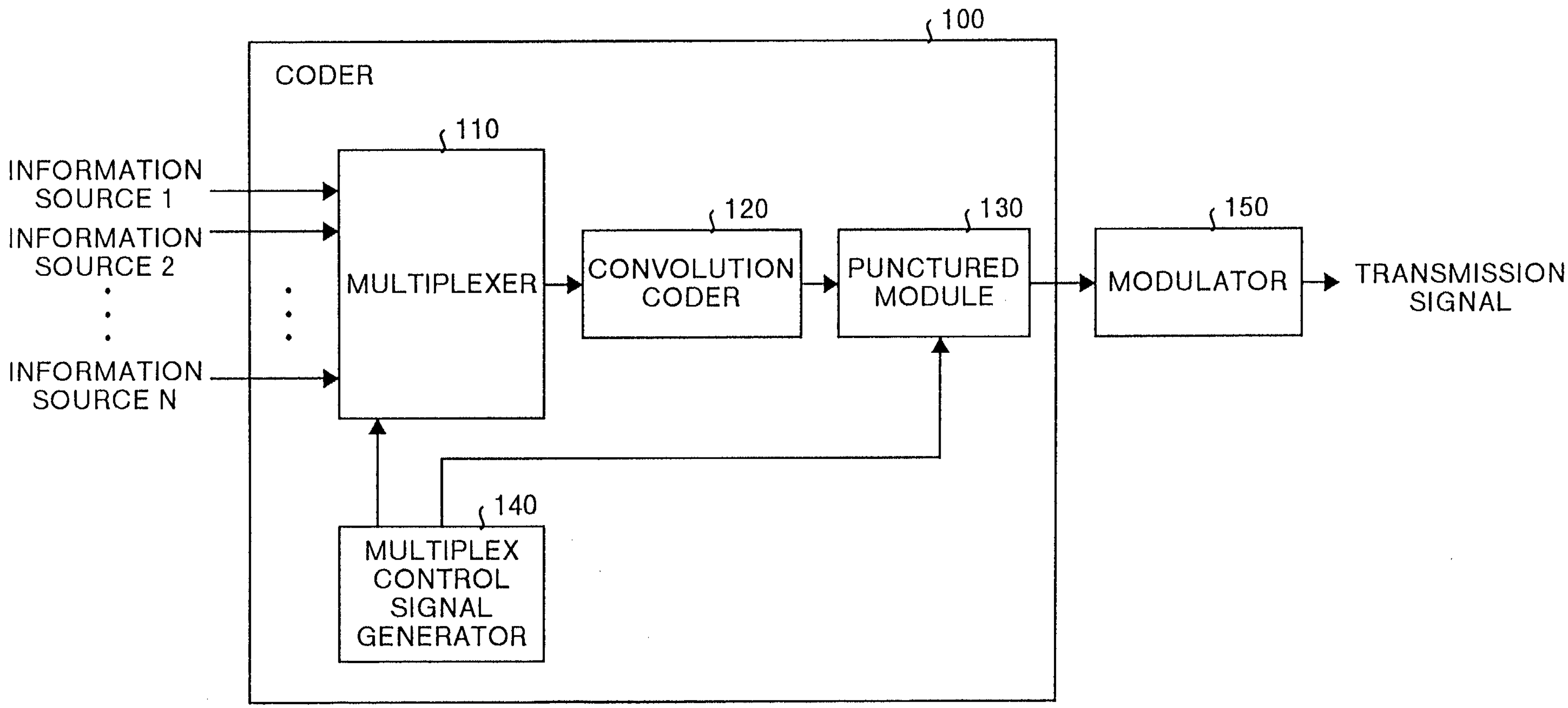

100
CODER
110
MULTIPLEXER
120
CONVOLUTION CODER
130
PUNCTURED MODULE
140
MULTIPLEX CONTROL SIGNAL GENERATOR
150
MODULATOR
TRANSMISSION SIGNAL
INFORMATION SOURCE 1
INFORMATION SOURCE 2
INFORMATION SOURCE N

FIG.2

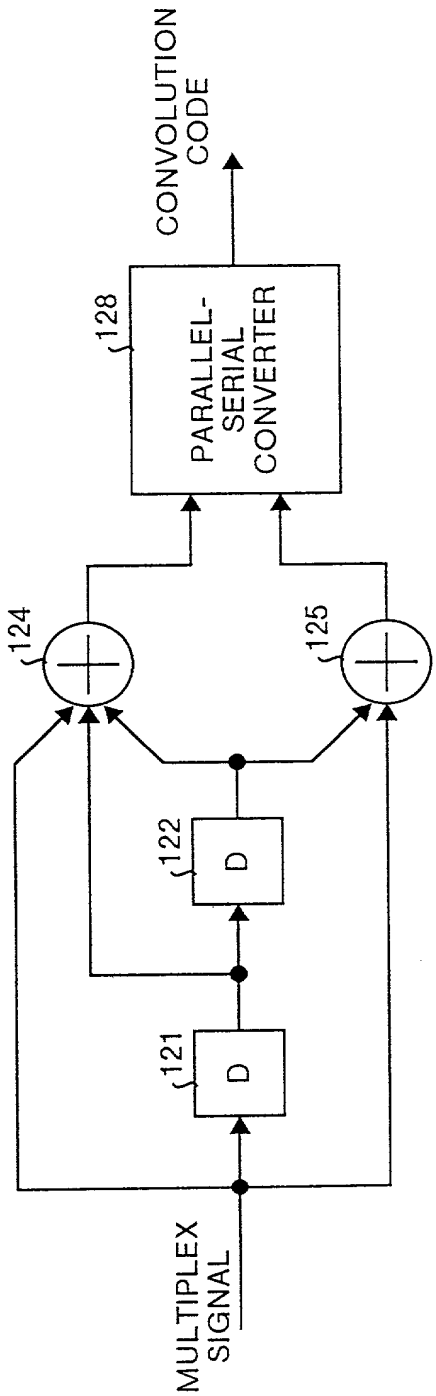
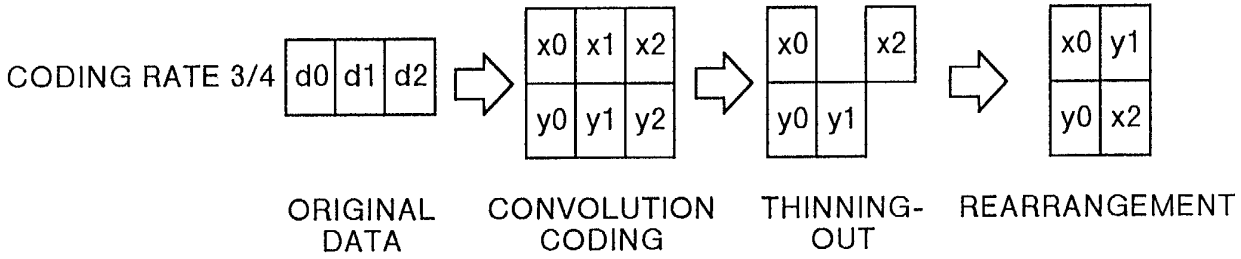
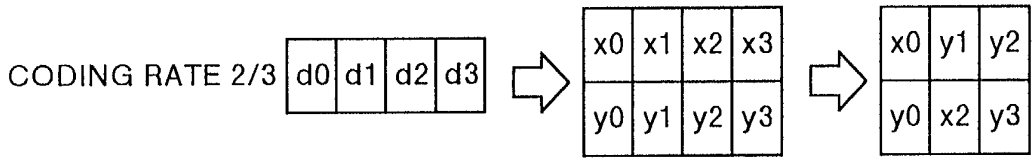
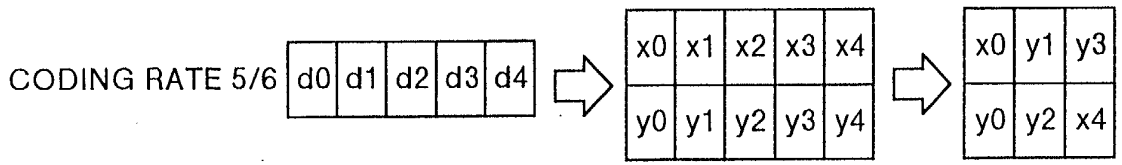

120
128
PARALLEL-SERIAL CONVERTER
CONVOLUTION CODE
124
125
122
D
121
D
MULTIPLEX SIGNAL

FIG.3







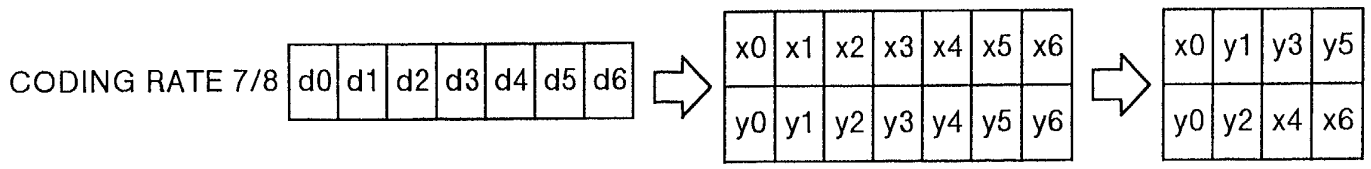


FIG.4

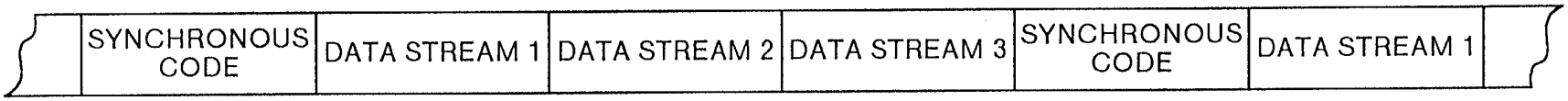


FIG.5

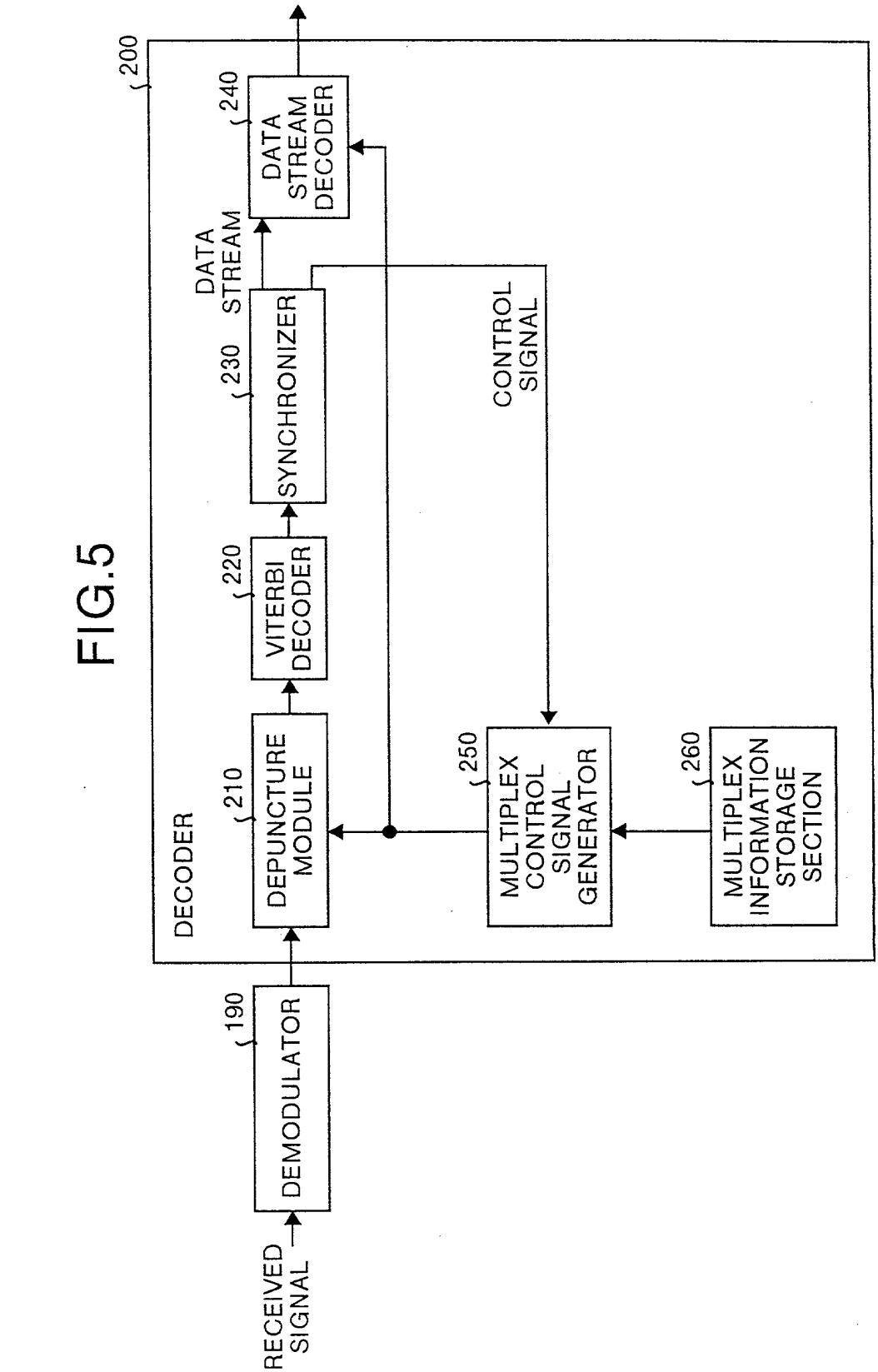

RECEIVED SIGNAL
190
DEMODULATOR
200
DECODER
210
DEPUNCTURE MODULE
220
VITERBI DECODER
230
SYNCHRONIZER
DATA STREAM
240
DATA STREAM DECODER
250
MULTIPLEX CONTROL SIGNAL GENERATOR
260
MULTIPLEX INFORMATION STORAGE SECTION
CONTROL SIGNAL

FIG.6

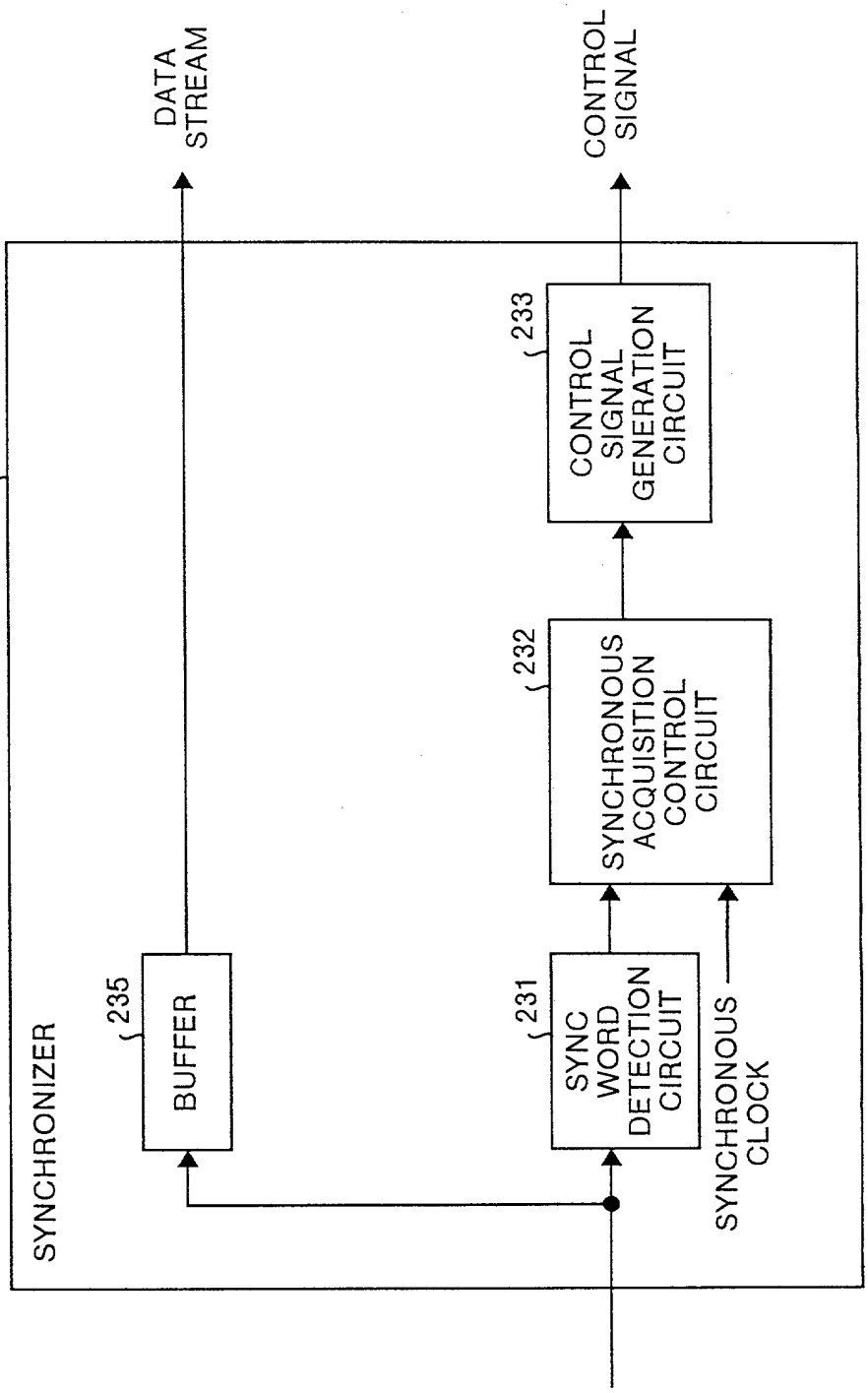

DATA STREAM
CONTROL SIGNAL
230
SYNCHRONIZER
233
CONTROL SIGNAL GENERATION CIRCUIT
232
SYNCHRONOUS ACQUISITION CONTROL CIRCUIT
235
BUFFER
231
SYNC WORD DETECTION CIRCUIT
SYNCHRONOUS CLOCK

FIG.7

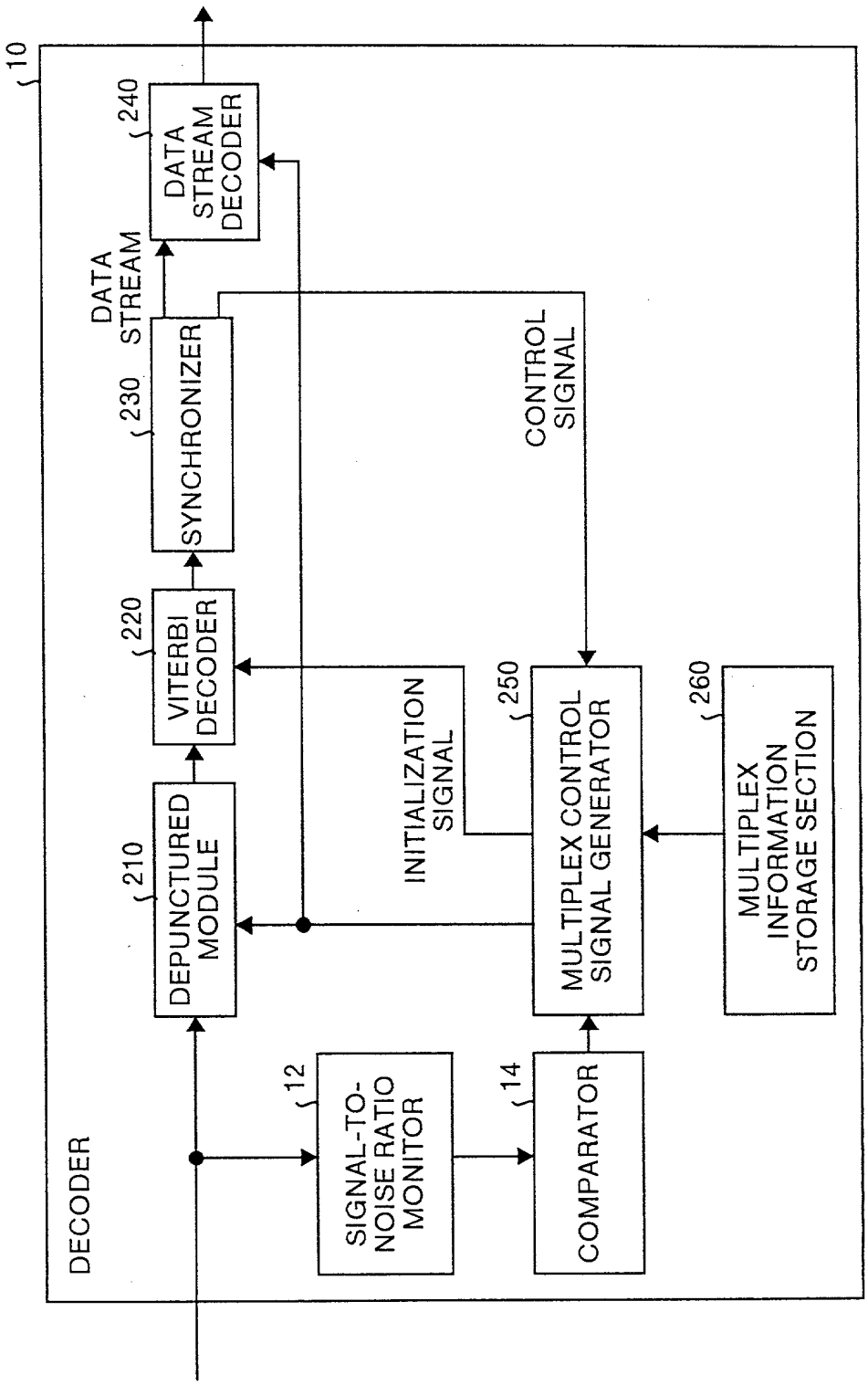

10
DECODER
12
SIGNAL-TO-NOISE RATIO MONITOR
14
COMPARATOR
210
DEPUNCTURED MODULE
220
VITERBI DECODER
230
SYNCHRONIZER
240
DATA STREAM DECODER
DATA STREAM
INITIALIZATION SIGNAL
250
MULTIPLEX CONTROL SIGNAL GENERATOR
260
MULTIPLEX INFORMATION STORAGE SECTION
CONTROL SIGNAL

FIG.8

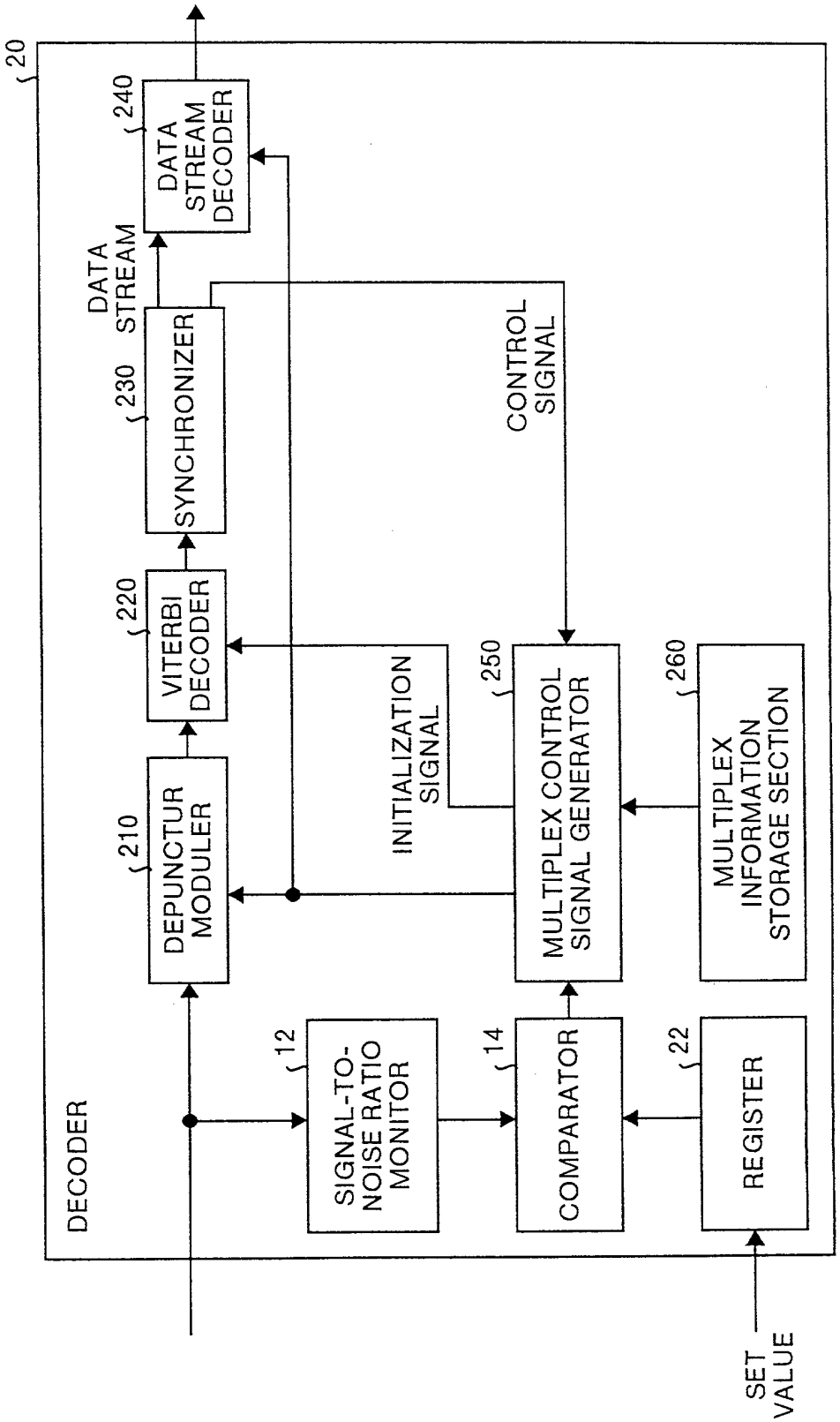

20
DECODER
210
DEPUNCTUR MODULER
220
VITERBI DECODER
230
SYNCHRONIZER
240
DATA STREAM DECODER
DATA STREAM
12
SIGNAL-TO-NOISE RATIO MONITOR
14
COMPARATOR
22
REGISTER
INITIALIZATION SIGNAL
250
MULTIPLEX CONTROL SIGNAL GENERATOR
260
MULTIPLEX INFORMATION STORAGE SECTION
CONTROL SIGNAL
SET VALUE

FIG.9

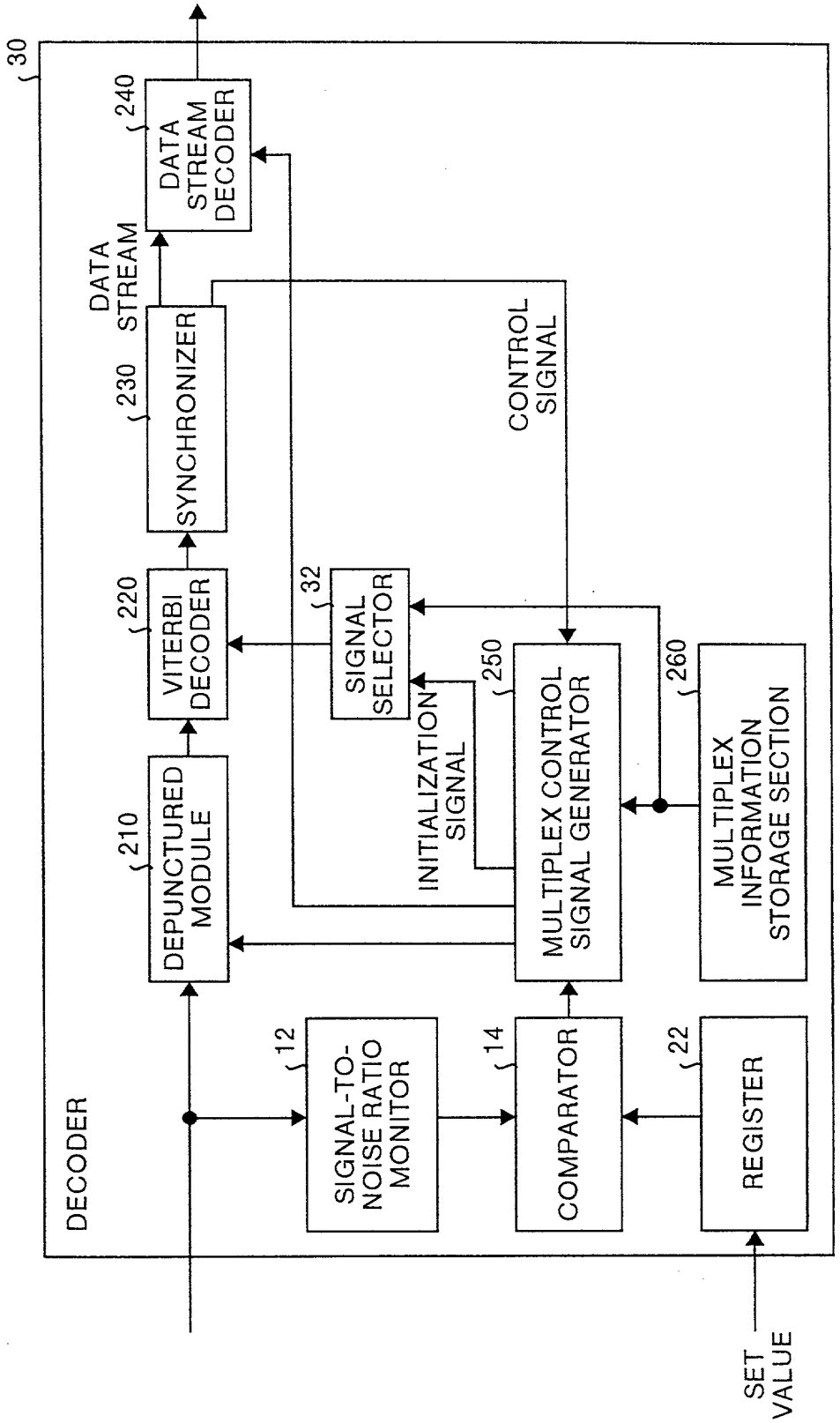

30
DECODER
210
DEPUNCTURED MODULE
220
VITERBI DECODER
230
SYNCHRONIZER
240
DATA STREAM DECODER
DATA STREAM
32
SIGNAL SELECTOR
INITIALIZATION SIGNAL
250
MULTIPLEX CONTROL SIGNAL GENERATOR
CONTROL SIGNAL
260
MULTIPLEX INFORMATION STORAGE SECTION
12
SIGNAL-TO-NOISE RATIO MONITOR
14
COMPARATOR
22
REGISTER
SET VALUE

FIG.10

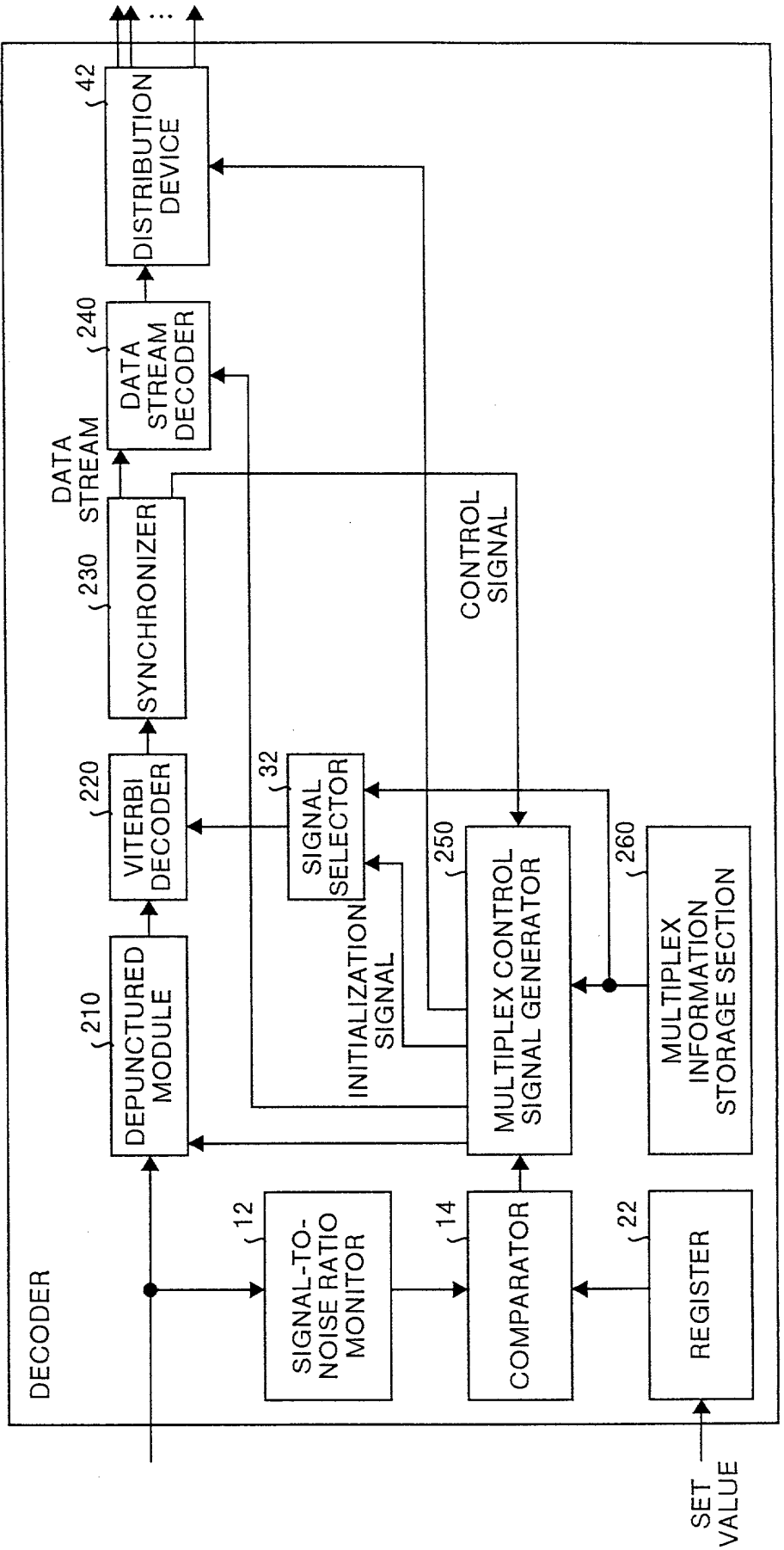

40
DECODER
42
DISTRIBUTION DEVICE
240
DATA STREAM DECODER
DATA STREAM
230
SYNCHRONIZER
CONTROL SIGNAL
220
VITERBI DECODER
32
SIGNAL SELECTOR
210
DEPUNCTURED MODULE
INITIALIZATION SIGNAL
250
MULTIPLEX CONTROL SIGNAL GENERATOR
260
MULTIPLEX INFORMATION STORAGE SECTION
12
SIGNAL-TO-NOISE RATIO MONITOR
14
COMPARATOR
22
REGISTER
SET VALUE

FIG.11

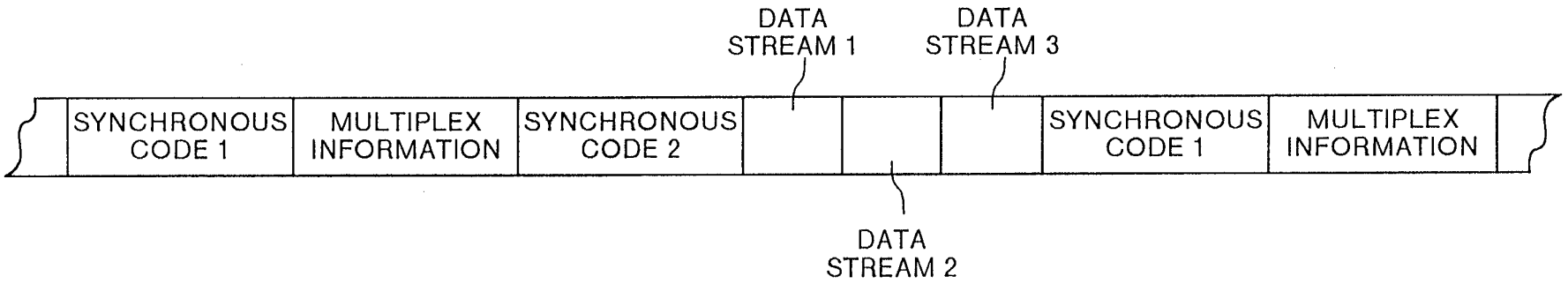
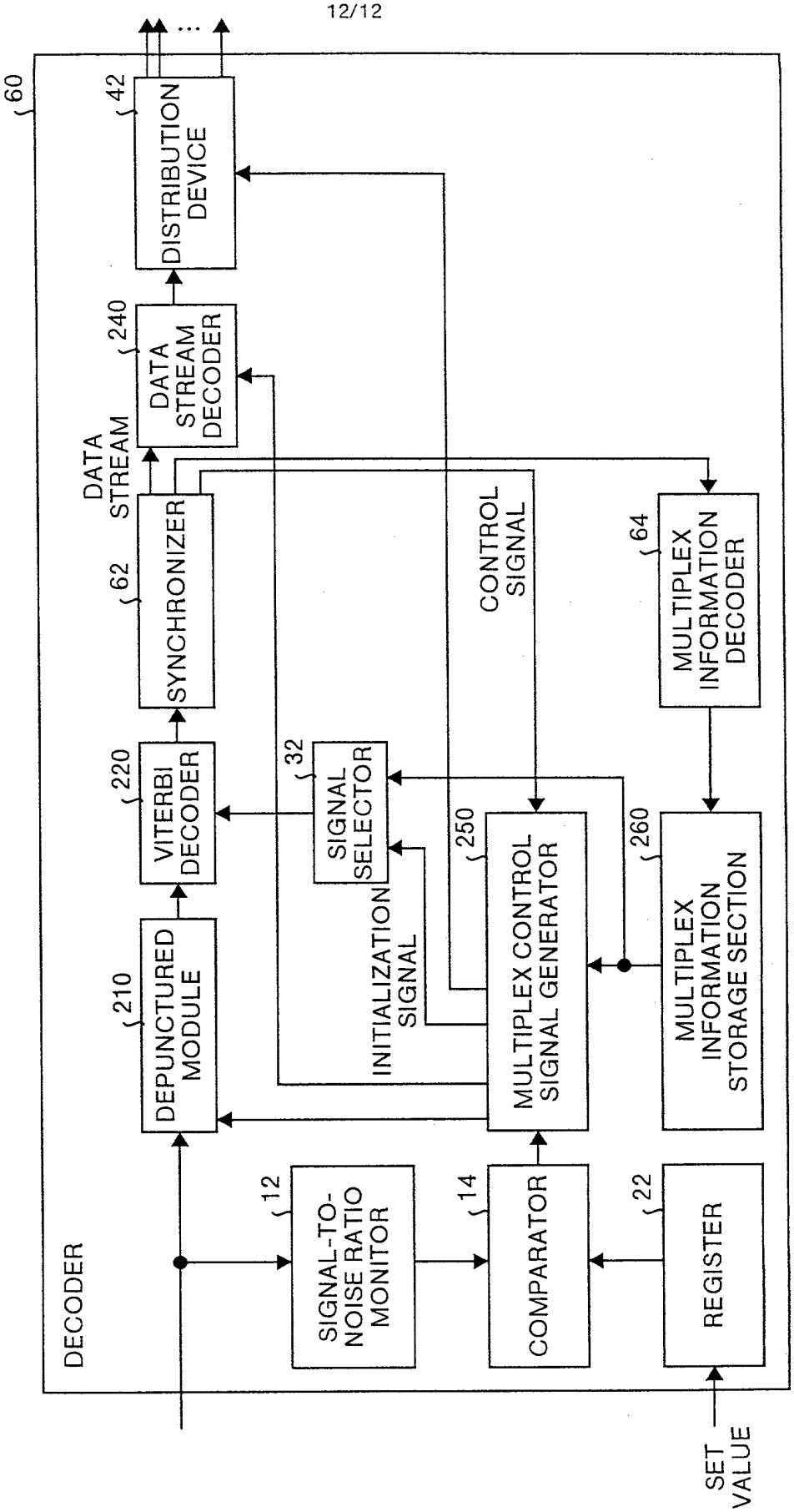


FIG.12


60
DECODER
42
DISTRIBUTION DEVICE
240
DATA STREAM DECODER
DATA STREAM
62
SYNCHRONIZER
220
VITERBI DECODER
32
SIGNAL SELECTOR
210
DEPUNCTURED MODULE
INITIALIZATION SIGNAL
CONTROL SIGNAL
250
MULTIPLEX CONTROL SIGNAL GENERATOR
260
MULTIPLEX INFORMATION STORAGE SECTION
64
MULTIPLEX INFORMATION DECODER
12
SIGNAL-TO-NOISE RATIO MONITOR
14
COMPARATOR
22
REGISTER
SET VALUE

99-2403

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
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Japanese Language Declaration

日本語宣言書

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As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR DECODING THE DATA, DATA RECEIVING SYSTEM, AND DATA TRANSMITTING AND RECEIVING SYSTEM

上記発明の明細書（下記の欄でX印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ＿月＿日に提出され、米国出願番号または特許協定条約国際出願番号を＿＿＿＿＿＿とし、
（該当する場合）＿＿＿＿＿＿ に訂正されました。

☐ was filed on ＿＿＿＿＿＿
as United States Application Number or
PCT International Application Number
＿＿＿＿＿＿ and was amended on
＿＿＿＿＿＿ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Approved for use through 9/30/98 OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Japanese Language Declaration
(日本語宣言書)

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
11-259315	Japan	13/September/1999	□
			□

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I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

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I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

And I hereby appoint as principal attorneys: David T. Nikaido, Reg. No. 22,663; Charles M. Marmelstein, Reg. No. 25,895; George E. Oram, Jr., Reg. No. 27,931; Robert B. Murray, Reg. No. 22,980; E. Marcie Emas, Reg. No. 32,131; Douglas H. Goldhush, Reg. No. 33,125; Monica Chin Kitts, Reg. No. 36,105; Richard J. Berman, Reg. No. 39,107; King L. Wong, Reg. No. 37,500; Karen K. Costantino, Reg. No. 35,107; James A. Poulos, III, Reg. No. 31,714; Patrick D. Muir, Reg. No. 37,403; Sharon N. Klesner, Reg. No. 36,335; and Murat Ozgu, Reg. No. 44,275; Bradley D. Goldizen, Reg. No. 43,637; and N. Alexander Nolte, Reg. No. 45,689.

書類送付先

直接電話連絡先： （名前及び電話番号）

Please direct all communications to the following address:
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 600
Washington, D.C. 20036-5339
Tel: (202) 857-6000; Fax: (202) 857-6395

唯一または第一発明者名	Full name of sole or first inventor Ken YAMAUCHI
発明者の署名 日付	Inventor's signature Date Ken Yamauchi July 24, 2000
住所	Residence Kawasaki, Japan
国籍	Citizenship Japanese
私書箱	Post Office Address c/o FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8588 Japan
第二共同発明者名	Full name of second joint inventor, if any
第二共同発明者の署名 日付	Second inventor's signature Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)